MULTI-CORE PROCESSORS: CONCEPTS AND IMPLEMENTATIONS

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ABSTRACT

This research paper aims at comparing two multi-core processors machines, the Intel core i7-4960X processor (Ivy Bridge E) and the AMD Phenom II X6. It starts by introducing a single-core processor machine to motivate the need for multi-core processors. Then, it explains the multi-core processor machine and the issues that rises in implementing them. It also provides a real life example machines such as TILEPro64 and Epiphany-IV 64-core 28nm Microprocessor (E64G401). The methodology that was used in comparing the Intel core i7 and AMD phenom II processors starts by explaining how processors' performance are measured, then by listing the most important and relevant technical specification to the comparison. After that, running the comparison by using different metrics such as power, the use of Hyper-Threading technology, the operating frequency, the use of AES encryption and decryption, and the different characteristics of cache memory such as the size, classification, and its memory controller. Finally, reaching to a roughly decision about which one of them has a better over all performance.

KEYWORDS

Single-core processor, multi-core processors, Intel core i7, AMD phenom, Hyper-Threading.

1. INTRODUCTION

1.1. Single-Core Processesor

A single-core processor machine as shown in Figure 1, consists of one processor, two or more levels of cache memory, main memory, hard disk, and Input/Output (I/O) devices. Levels of cache relates to the size and distance from the processor as shown in Figure 2 which displays the memory hierarchy, for example accessing data from Level 1 (L1) cache is faster than accessing it from L2 cache, and so on. Consequently, the use of cache memory reduces the Memory Access Time (MAT) resulting in a better performance.

According to Moor's law that was stated in 1965, the number of transistors on a chip will roughly double each year, then he refined the period in 1975 to be two years. Moore's law is often quoted as Dave House's revision that computer performance will double every 18 months [3]. The problem of adding more transistors on a chip in the amount of generated heat that exceeds the advancements rate of the cooling techniques which is known as “the power wall” problem [7].

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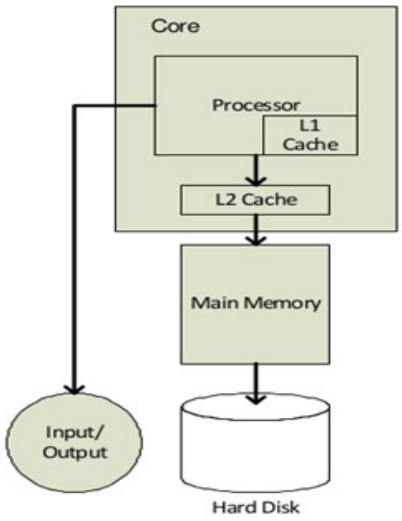

Figure 1. Single-core processor machine [3]

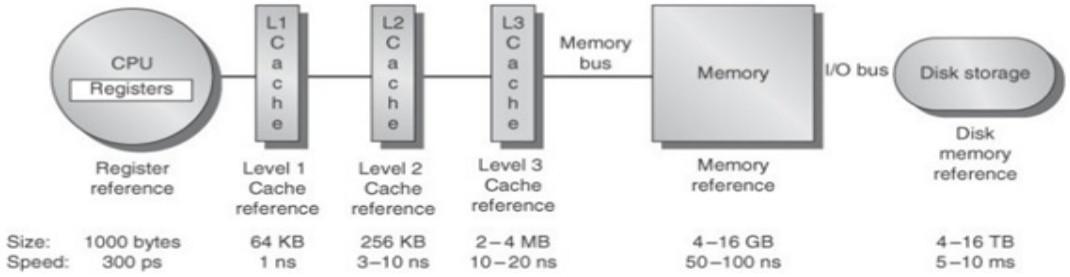

Figure 2. Memory hierarchy [7]

1.2. Multi-core processesor

A multi-core processor is an integrated circuit (IC) to which two or more processors have been attached for enhanced performance, reduced power consumption, and more efficient simultaneous processing of multiple tasks, it is a growing industry trend as single-core processors rapidly reach the physical limits of possible complexity and speed [1]. A basic block diagram of a generic multi-core processor is shown in Figure 3.

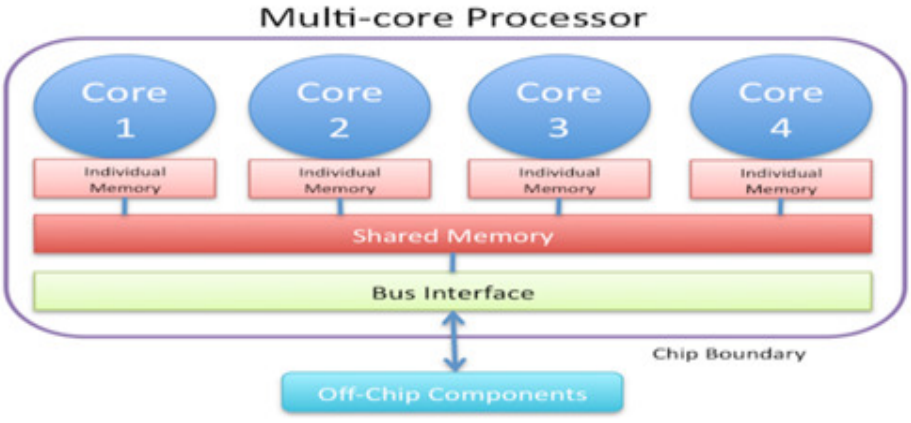

Figure 3. Block diagram for a general Multi-Core processor [2]

The high performance demand of users also motivated the shift from single-core to multi-core processors. A comparison between a single-core and a multi-core processors that occupies the same die area is shown in Figure 4.

	Single core processor (45nm)	Multi-core processor (45nm)
Vdd	1.0V	1.0V
I/O pins(total)	1280 (ITRS)	3000 (Estimated)
Operating frequency	7.8GHz	4GHz
Chip-package data rate	7.8 Gb/s	4Gb/s
Bandwidth	125GByte/s	1 TeraByte/s
Power	429.78W	107.39W
Total number of pins on chip	3840	9000(Estimated)
Number of pins on the package	2480	4500(Estimated)

Figure 4. A comparison between single-core vs. multi-core processors [3]

2. ISSUES IN DEVELOPING MULTI-CORE PROCESSORS MACHINES

The first issue is the communication between core processors and the main memory in a multi-core processors' environment. This is done either by the use of a single communication bus “shared memory model” or an interconnection network “distributed memory model” as shown in Figure 5. The single bus approach has an upper limit of 32 cores, after that the bus will be overfilled with transactions that lower the performance of the system [3].

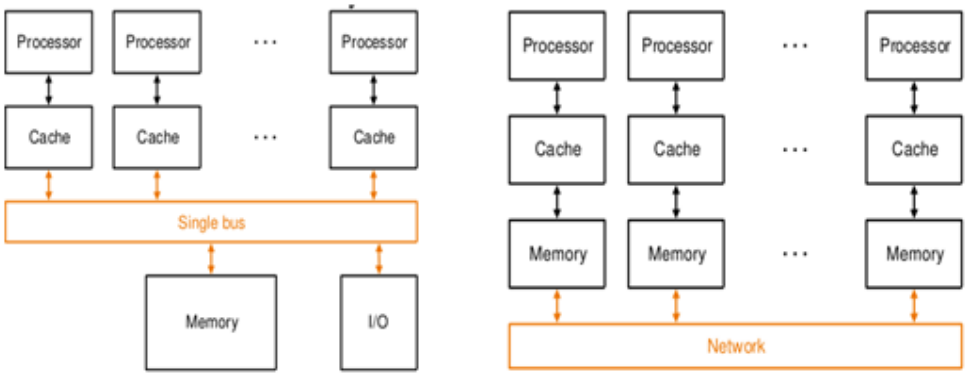

Figure 5. Shared memory approach (right) vs. distributed memory model (left)

Since every core processor has its own memory in the distributed memory model, a copy of the data might not be always the most updated version, which will result in a cache coherence problem. For example, if we have a dual core processor, each core will get a portion of the memory, if the first core writes a new value for a parameter and the second core had to read the value of this parameter it will read its own value unless there is a coherence policy. Rreading a non consistent value of this parameter may result in a program crash. There are two schemes that forces cache coherence, the snooping protocol and a directory protocol. The snooping protocol is

designed only for a bus based system, it uses a number of states to determine whether or not there is a need to update the cache entries or not and also if it has control over writing to the block. However, the directory protocol has the scalability to work on any arbitrary network. A directory is used to hold information about which of the memory locations are being used exclusively by one core, and which are shared among multiple cores [3].

The second issue that rise in order to fully utilize the multi-core processor technology is parallelism, programs should have the characteristic of being executed in a parallel order. There are three types of parallelism: Instruction level parallelism, thread level parallelism, and data level parallelism. In the case of Instruction level parallelism, the execution of the instructions could be done in a parallel way as well as in a sequential way. In the case of thread level parallelism, multiple threads of the same task are presented to the processor to be executed simultaneously as shown in Figure 6. In the case of data level parallelism, common data is being shared among executing processes through memory coherence, which will improve performance by reducing the time required to load and access memory [2]. However, according to Amdahl's law the performance of Parallel applications in a multi-core environment is limited by its non-parallel part that form bottlenecks. So, for an optimal use of the multi-core processors the non-parallel part has to be optimized by either parallelizing the non-parallel part or by making them faster using more efficient algorithms [4].

Starvation is a problem that could occur if the program isn't designed in a parallel way, this is because one or more cores might starve for data. For example, if a single-threaded application is to be run in a multi-core processor machine. The thread will run in one of the cores while the other cores remains idle. Another example could be seen in a multi-core processor machine with a shared cache such as the Intel Core 2 Duo's shared L2 cache, unless a proper replacement policy was placed one core may starve for cache usage and keeps making a costly calls out to main memory. The replacement policy should have a mechanism for ejecting cache entries that other cores have recently loaded. In the case where the number of cores is large, applying this replacement policy becomes difficult to reduce the amount of ejected cache space without increasing cache misses [3].

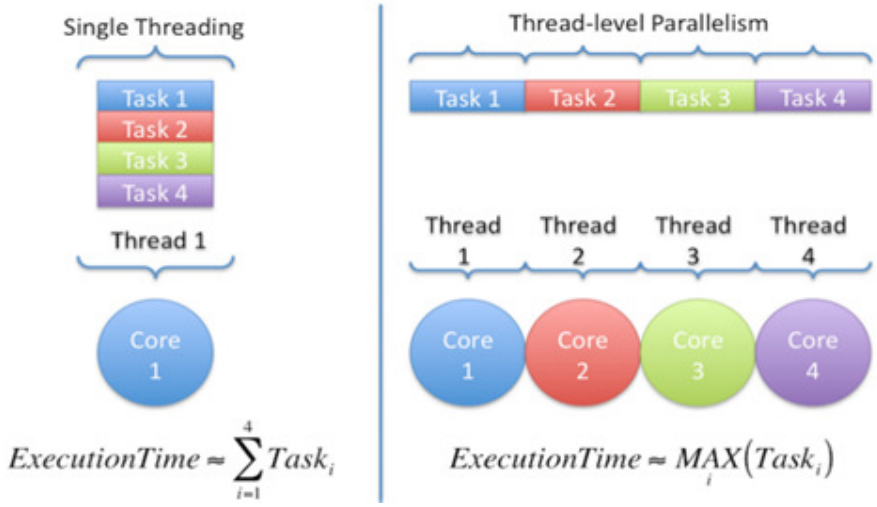

Figure 6. Thread level parallelism [2]

The third issue that rise in the development of multi-core processors is power dissipation. If we allocate two cores on the same chip size a large amount of heat will be generated unless there is a power control mechanism that shuts down the unused core or limits its power consumption [3].

Finally, the fourth issue that rise in the development of multi-core processors is whether to use homogeneous or heterogeneous cores. Homogeneous cores are all exactly the same, they run on an equivalent frequencies, have the same cache sizes and functionalities. However, heterogeneous cores are different in their frequencies, memory models and functionalities. The choice will be based on making a trade-off between processor complexity and customization. The production of homogeneous cores are easier since all cores contains the same hardware and use the same instruction set. While in the case of heterogeneous cores, each core could have a specific function and run its own specialized instruction set. For example, the CELL processor has heterogeneous cores, one Power Processing Element (PPE) and eight Synergistic Processing Elements (SPE). The PPE core is used as a large centralized processing unit, while the other PPEs are used for different functionalities such as graphics, communications, enhanced mathematics, audio, and so on. The heterogeneous model is more complex, but may have efficiency, power, and thermal benefits that outweigh its complexity [3].

3. EXAMPLES OF MULTI-CORE PROCESSORS MACHINES

3.1. TILEPRO64

This multi-core processors machine has 64 homogeneous cores that are arranged in a mesh network. Each core consists of a full-featured processor, L1 and L2 cache, and a non-blocking switch that connect the core with the whole mesh. The Tile pro family incorporates Tilera's Dynamic Distributed Cache (DDC) technology which accelerates the cache coherence performance by a factor of two when compared to other multi-core processors machines. The TIELPro64 has many attractive features such as the massively scalable performance, power efficiency, and it is considered as an Integrated solution. Its processor cores combines the features of a general-purpose Central Processing Unit (CPU) along with a powerful signal processing and Single Instruction, Multiple Data (SIMD) capabilities, which will result in integrating multiple functionalities on the same single processor that reduces the system cost and simplifies the system design. It uses a 32-bit Very Long Instruction Word (VLIW) processors with 64-bit instruction bundle, and its pipeline has a 3-deep pipeline with up to 3 instructions per cycle resulting in executing 12 times the instructions if compared to a single-core. Its on-chip cache size 5.6 Mbytes, executes up to 443 billion operations per second (BOPS), and 200 Gbps memory bandwidth with four 64-bit DDR2 controllers [6]. If VLIW is combined with the MIMD (multiple instruction, multiple data) processors, multiple operating systems could be run in a simultaneous order and advanced multimedia applications such as video conferencing and video-on-demand could be run more efficiently [3].

3.2. EPIPHANY-IV 64-CORE 28NM MICROPROCESSOR (E64G401)

This multi-core processors machine has 64 High Performance Reduced Instruction Set Computer (RISC) CPU Cores arranged in a 8 * 8 mesh network, each core operates at 800 MHz and 1.6 GFLOPS/sec. The CPU has an efficient general-purpose instruction set that excels at compute intensive applications while being efficiently programmable in C/C++ without any need to write code using assembly or processor specific intrinsics [8].

This machine's memory architecture is based on a flat memory map in which each compute node has a small amount of local memory as a unique addressable slice of the total 32-bit address space. A processor can access its own local memory and other processors memory through regular load/store instructions, with the only difference being the latency and effective throughput of the transactions. The local memory system is comprised of 4 separate banks, allowing for simultaneous memory access by the instruction fetch engine, local load-store instructions, and by load/store transactions initiated by other processors within system [8].

4. PERFORMANCE MEASUREMENT OF A PROCESSOR

There are many metrics which could be used in measuring processors performance such as: throughput which is the average rate of how many processes were executed successfully; response time which is the time between the time between the request time and time that the system starts working on this request; execution time which is the time needed to finish the request, energy consumption, and the memory bandwidth which is the rate of data sustained from the CPU core to the RAM. All these metrics could be classified into three main categories: higher is better, lower is better, and nominal is better. For example, higher throughput is better, lower execution time is better, and nominal power consumption is better [5].

5. COMPARING TWO MULTI-CORE PROCESSORS MACHINES

In this section a comparison between two multi-core processors machines will be made, the Intel core i7-4960X processor (Ivy Bridge E) and the AMD Phenom II X6 processor.

5.1. INTEL CORE I7-4960X PROCESSOR (IVY BRIDGE E)

Intel uses a naming scheme for its Core processors, the three brands are, Core i3, Core i5 and Core i7, these brand names aren't related to specific technical features such as the number of cores. Instead, they correspond to three, four and five stars in Intel's Intel Processor Rating from low-level (Core i3), through mid-range (Core i5) to high-end performance (Core i7), following on from the entry-level Celeron (one star) and Pentium (two stars) processors. The Intel brand name of Intel Core i7 applies to several families of desktop and laptop 64-bit x86-64 processors using the Nehalem, Westmere, Sandy Bridge, Ivy Bridge and Haswell micro architectures. Both the regular Core i7 and the Extreme Edition are advertised as five stars in the Intel Processor Rating [9]. A comparison of the Core i7 family can be found in [10].

One of Intel's latest Core i7 models in the market is the Core i7-4960X processor (Ivy Bridge E), its die details' diagram can be found in [10] , and its technical specifications are [11][15]:

- 6 cores
- 12 threads
- Clock speed of 3.6 GHz
- Max turbo frequency is 4 GHz
- Level 1 cache (32 KB (code) / 32 KB (data)) per core
- Level 2 cache 256 KB
- Level 3 cache 15360 KB shared for all cores
- Instruction set of 64 bits
- Thermal Design Power (TDP) of 130W
- Max Temperature is 66.8 C
- Introduction date (September 10, 2013)
- Die size is 22nm
- supports 4 memory channels
- supports DDR3-1066, DDR3-1333, DDR3-1600, DDR3-1866

5.2. AMD PHENOM II X6 1100T

Phenom II is a family of AMD's multi-core 45nm processors using the AMD K10 micro architecture, succeeding the original Phenom. Advanced Micro Devices released the Socket

AM2+ version of Phenom II in December 2008, while Socket AM3 versions with DDR3 support, along with an initial batch of triple- and quad-core processors were released on February 9, 2009. Dual-processor systems require Socket F+ for the Quad FX platform. The second-generation of Phenom II X6 was released on April 27, 2010 [12].

One of the latest AMD Phenom processors in the market is AMD Phenom II X6 1100T, its technical specifications are [13][15]:

- 6 cores
- 6 threads
- Clock speed of 3.3 GHz
- Max turbo frequency is 3.7 GHz
- Level 1 cache (64 KB (code) / 64 KB (data)) per core
- Level 2 cache 512 KB per core
- Level 3 cache 6144 KB shared for all cores
- Instruction set of 64 bits
- Thermal Design power of 125W
- Max Temperature is 62 C
- Die size 45nm
- supports 2 memory channels
- supports DDR2-1066, DDR3-1333

5.3. COMPARISON METRICS

The first metric of comparison is based on power, the Phenom II X6 1100T saves 4% more energy than the Core i7-4960 X. This is shown in Figure 7.

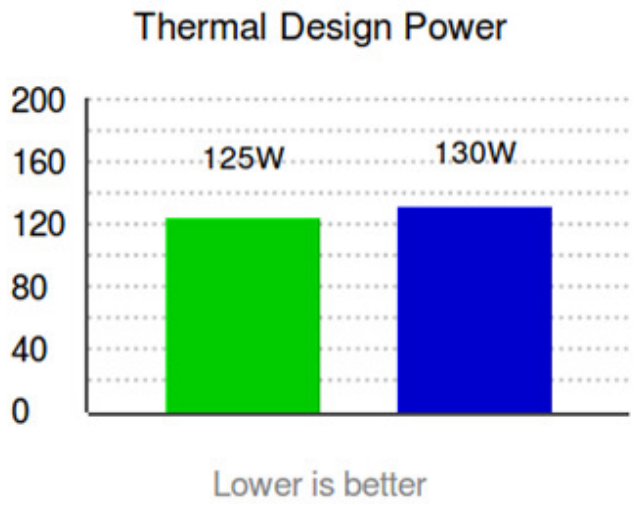

Figure 7. Power Comparison, AMD in green and Intel in blue [15]

The second metric of comparison is based on Hyper-Threading technology, Intel Core i7-4960X enables the Hyper-Threading technology, while the AMD Phenom II X6 does not. This will allow the Intel Core i7 microprocessor to execute twice as many threads. This is shown in Figure 8.

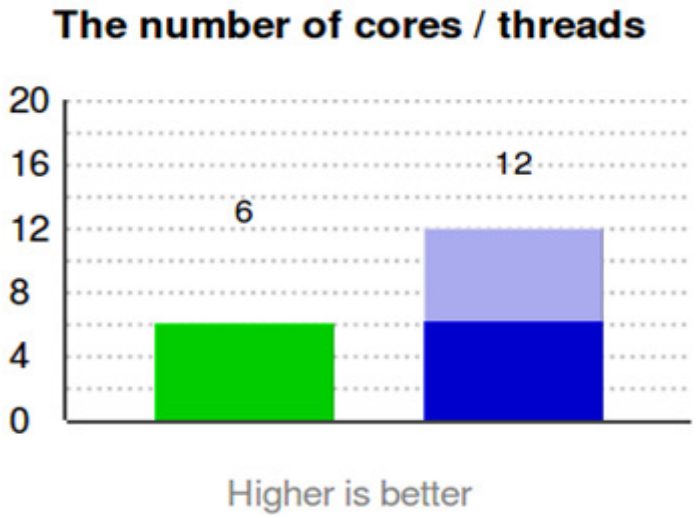

Figure 8. Cores/threads comparison, AMD in green and Intel in Blue, the number of cores (darker area). Lighter area on the graph represents the number of additional threads, offered by Hyper-Threading technology [15].

The third metric of comparison is based on the operating frequency, the Intel Core i7-4960X has a higher frequency than the AMD of the 1100T. This will allow it to execute more operations per minute. This is shown in Figure 9.

Figure 9. Operating frequency comparison, AMD in green and Intel in blue, the dark color for base frequency, while lighter area is for extra frequency, provided by Turbo feature [15].

The fourth metric is based on the AES encryption and decryption, the Intel Core i7-4960X incorporates Advanced Encryption Standard (AES) technology. This extension provides hardware acceleration of AES encryption and decryption, and is useful if you run programs, that protect your disk or network data [15].

The fifth metric of comparison is based on cache memory size, this is shown in Figure 10.

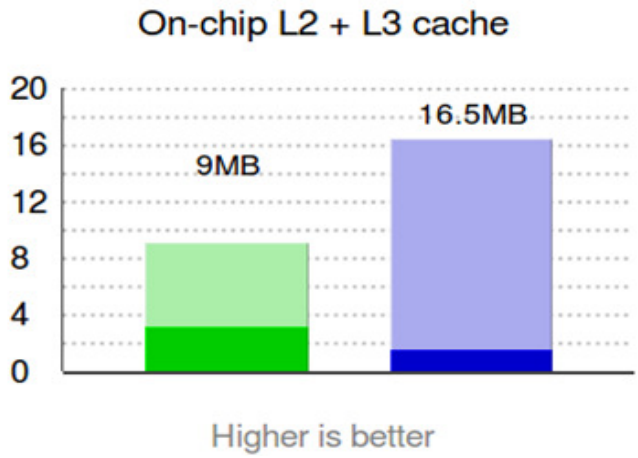

Figure 10. Cache memory size comparison, AMD in green and Intel in blue, darker area on the "On-chip cache" graph is for the On-chip L2 cache. Lighter area is for the L3 cache cache [15].

The sixth metric of comparison is based on the classification of the cache memory, Intel's Core i7's cache memory is an inclusive cache while in the case of the AMD it is exclusive. Inclusive cache means that all the data that are stored in each individual L1 and L2 will be duplicated. This duplication will greatly improve the inter-core communication because any given core does not have to locate data in another processor's cache. If for example the requested data was not found in any level of the core's cache, this will give an indicator to all the other cores that the data is not present in any other core's cache. In addition, Intel core i7 uses a Translation Look-aside Buffer (TLB) which plays a critical role in the cache performance. The TLB is a high-speed buffer that maps virtual addresses to physical addresses in the cache. The advantage of using the TLB is to quickly access a page memory when it is mapped in the TLB. In addition, Intel made the TLB dual-level by adding an L2 TLB. The second-level TLB is larger than the first level and can store up to 512 entries. As a result of these and other design differences, including a remapped TLB hierarchy, the Core i7's cache latencies are much lower than the Phenom's [16].

The seventh metric of comparison is the memory controller, the Core i7 integrated memory controller allows it to get to main memory very quickly, which eliminates the chip-to-chip "hop" required when going over a front-side bus to an external north bridge. Again, this is a familiar page from AMD's template, but Intel has raised the stakes by incorporating support for three channels of DDR3 memory. With the memory controller on-board and the front-side bus gone, the Core i7 communicates with the rest of the system via the QuickPath interconnect, or QPI. QuickPath is Intel's answer to HyperTransport, a high-speed, narrow, packet-based, point-to-point interconnect between the processor and the I/O chip (or other CPUs in multi-socket systems.) The QPI link on the Core i7-965 Extreme operates at 6.4 GT/s. At 16 bits per transfer, that adds up to 12.8 GB/s, and since QPI links involve dedicated bidirectional pairs, the total bandwidth is 25.6 GB/s. Lower-end Core i7 processors have 4.8 GT/s QPI links with up to 19.2 GB/s of bandwidth. Still, both are somewhat faster than the HyperTransport 3 interconnects in today's Phenoms, which peak at either 16 or 14.4 GB/s, depending on the chip [17].

6. CONCLUSION

According to the comparison that has been made based on different metrics, each processor had its advantages and drawbacks. The AMD Phenom outperformed Intel core i7 in L1 and L2 cache memory size and its cheaper. The Intel core i7 outperformed the AMD in many other metrics such as power saving, the use of Hyper-Threading technology, smaller die size, higher operating frequency, AES encryption and decryption, larger L3 cache memory, the use of inclusive cache

memory has a better performance than the use of exclusive cache memory as in the AMD phenom processor, and also a better memory controller. Based on all these results, a recommendation could be made to use the Intel core i7 if a higher performance is needed and the budget can allow the extra cost.

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